REMARKS

The present application was filed on May 30, 2001 with claims 1-41. Applicant filed a Response to Restriction Requirement on March 20, 2002, electing claims 1-7, 36, 37, 40 and 41 for prosecution on the merits. Claims 8-35, 38 and 39 are withdrawn from consideration.

In the outstanding Office Action dated April 25, 2002, the Examiner rejected claims 1-7, 36, 40 and 41 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,901,087 (hereinafter "Pascucci"), and rejected claim 37 under 35 U.S.C. §103(a) as being unpatentable over Pascucci.

In this response, Applicant traverses the §102(b) and §103(a) rejections, and amends independent claim 40.

With regard to independent claims 1, 36 and 37, each of these claims calls for a comparator circuit having an evaluation element and first and second input legs coupled thereto, with the first and second input legs being adapted to receive respective first and second input signals, and with the evaluation element being adapted to perform a comparison of the first and second input signals. Applicant respectfully submits that such an arrangement is not taught or suggested by the Pascucci reference. More particularly, as will be described below, Pascucci fails to teach or suggest an arrangement in which an evaluation element is adapted to perform a comparison of first and second input signals applied to respective first and second input legs as claimed.

The Examiner in formulating the §102(b) and §103(a) rejections argues that the claimed evaluation element corresponds to virtual ground latch structure 2 of Pascucci FIG. 2, and that the claimed first and second input legs correspond to the respective left branch 8 and right branch 9 coupled to respective nodes B and B′ in Pascucci FIG. 2 (Office Action, page 2, section 3). The Examiner fails to identify the particular input signals in Pascucci which correspond to the claimed input signals. However, Pascucci indicates in FIG. 2 and the associated text that the input signals applied to each of the left branch 8 and right branch 9 comprise signals associated with 16-bit buses YM and YN. The buses YM and YN are each connected to both the left branch 8 and the right branch 9. Pascucci further indicates that the buses YM and YN collectively characterize a "selection means" which "provides the ability to select a memory cell from the memory cell matrix" comprising memory cells 16 and 17 (Pascucci, column 3, lines 34-43). The FIG. 2 circuit does not compare

input signals, but instead determines if particular ones of the memory cells 16 and 17 are programmed or unprogrammed (Pascucci, column 5, line 39 to column 6, line 3).

Applicant submits that the virtual ground latch structure 2, which the Examiner has characterized as corresponding to the claimed evaluation element, is not adapted to perform a comparison of any signals associated with the buses YM and YN. In other words, the input signals YM and YN shown in Pascucci FIG. 2 are not compared by the virtual ground latch structure 2. Moreover, there are no other input signals in Pascucci that are applied to left branch 8 and right branch 9 and which are compared by the virtual ground latch structure 2. Pascucci therefore fails to teach or suggest at least the limitation of claims 1, 36 and 37 regarding an evaluation element of a comparator circuit being adapted to perform a comparison of first and second input signals applied to respective first and second input legs. The §102(a) and §103(a) rejections are therefore believed to be improper, and should be withdrawn.

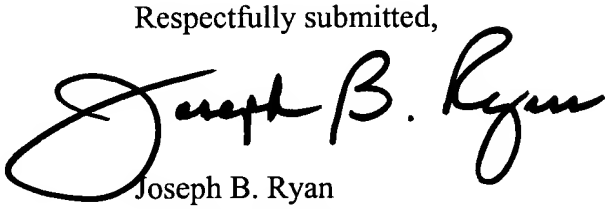
Dependent claims 2-7 are believed allowable for at least the reasons identified above with regard to their corresponding independent claim 1.

Independent claim 40 has been amended to specify that at least one of the first and second input legs comprises a weighted array of transistors, with each of the transistors in the weighted array adapted to receive a particular portion of an input signal applied to that leg. Support for the amendment can be found in the specification at, for example, page 18, lines 12-21. Such an arrangement is not taught or suggested by Pascucci or the other art of record.

Attached hereto is a marked-up version of the changes made to the claims by the present Amendment.

In view of the above, Applicant believes that claims 1-7, 36, 37, 40 and 41 are in condition for allowance, and respectfully requests withdrawal of the §102(b) and §103(a) rejections.

Respectfully submitted,



Date: September 25, 2002

Joseph B. Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

40. (Amended) A circuit comprising at least first and second input legs, the first and second input legs having non-complementary structures relative to one another, each of the non-complementary structures having associated therewith a variable parameter having a value that is a function of a corresponding input signal, a difference in the variable parameters associated with the first and second input legs being detectable in the circuit;

wherein at least one of the first and second input legs comprises a weighted array of transistors, each of the transistors in the weighted array adapted to receive a particular portion of an input signal applied to that leg.